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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,688	02/09/2006	Masaya Sumita	071971-0484	5369
53080 MCDERMOTT	7590 04/13/2007 Γ WILL & EMERY LLP		EXAMINER	
600 13TH STR	EET, NW		LE, THONG QUOC	
WASHINGTON, DC 20005-3096			ART UNIT	PAPER NUMBER
			2827	
SHORTENED STATUTOR	Y PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
3 MONTHS 04/13/2007		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)			
	10/567,688	SUMITA, MASAYA			
Office Action Summary	Examiner	Art Unit			
	Thong Q. Le	2827			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 16(a). In no event, however, may a reply be tim rill apply and will expire SIX (6) MONTHS from to cause the application to become ABANDONED	l. ely filed the mailing date of this communication. 0 (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on 2a) This action is FINAL . 2b) This 3) Since this application is in condition for allowant closed in accordance with the practice under Expression in the practice under Expression is the practice under Expression in the practice under	action is non-final. ace except for formal matters, pro				
Disposition of Claims					
4) Claim(s) 1-36 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1 is/are rejected. 7) Claim(s) 2-36 is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers 9) The specification is objected to by the Examiner 10) The drawing(s) filed on is/are: a) acceed to the proper and propers Application Papers 9) The specification is objected to by the Examiner and propers 10) The drawing(s) filed on is/are: a) acceed to the proper are properties. Application The oath or declaration is objected to by the Examiner and properties.	election requirement. r. epted or b) objected to by the Edrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	ected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) \(\sum \bigsigma^\text{Notice} \) of References Cited (PTO-892) 2) \(\sum \text{Notice} \) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) \(\sum \bigsigma^\text{Information Disclosure Statement(s)} \) (PTO/SB/08) Paper No(s)/Mail Date \(\frac{02/09/2006}{2006} \).	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:	te			

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DETAILED ACTION

1. Pre-amendment filed on 02/09/2006has been entered.

Claims 1-36 are presented for examination.

Information Disclosure Statement

- 2. This office acknowledges receipt of the following items from the Applicant:
 Information Disclosure Statement (IDS) filed on 02/09/2006.
- 3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ooi (U.S. Patent No. 5,043,878).

Regarding claim 1, Ooi discloses a semiconductor integrated circuit (Figure 1), comprising:

first and second information holding circuits (Figure 5, 413, 414) formed in a memory cell array for holding information (Column 2, lines 54-58);

a first port section (Figure 4, 437) for inputting or outputting information, which is connected only to the first information holding circuit;

a second port section (Figure 4, 438) for inputting or outputting information, which is connected only to the second information holding circuit; and

an interchange circuit (Figure 4, 111) receiving an interchange control signal for interchanging, in the memory cell array, information held in the first information holding circuit and information held in the second information holding circuit with each other (Column 4, lines 55-59).

8. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. (U.S. Patent No. 4,947,373).

Regarding claim 1, Yamaguchi et al. discloses a semiconductor integrated circuit (Figure 1), comprising:

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first and second information holding circuits (ABSTRACT) formed in a memory cell array for holding information (first register and second register, (Figure 1, DRA1, DRAB1);

a first port section (Figure 6, DRA1) for inputting or outputting information, which is connected only to the first information holding circuit;

a second port section (Figure 6, DRB1) for inputting or outputting information, which is connected only to the second information holding circuit; and

an interchange circuit (ABSTRACT, transfer means) receiving an interchange control signal for interchanging, in the memory cell array, information held in the first information holding circuit and information held in the second information holding circuit with each other.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Dolkas et al. (U.S. Patent No. 5,007,051).

Regarding claim 1, DOlkas et al. discloses a semiconductor integrated circuit (Figure 4), comprising:

first and second information holding circuits (ABSTRACT) formed in a memory cell array for holding information (Figure 4, 115, 113);

a first port section (ABSTRACT, first port means) for inputting or outputting information, which is connected only to the first information holding circuit;

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a second port section (ABSTRACT, second port means) for inputting or outputting information, which is connected only to the second information holding circuit; and

an interchange circuit (Figure 4, 131) receiving an interchange control signal for interchanging, in the memory cell array, information held in the first information holding circuit and information held in the second information holding circuit with each other (ABSTRACT).

10. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Taniai et al. (U.S. Patent No. 5,043,935).

Regarding claim 1, Taniai et al. discloses a semiconductor integrated circuit (Figure 1), comprising:

first and second information holding circuits (Figure 1, 4) formed in a memory cell array for holding information;

a first port section (Figure 1, 3a) for inputting or outputting information, which is connected only to the first information holding circuit;

a second port section (Figure 1, 3b) for inputting or outputting information, which is connected only to the second information holding circuit; and

an interchange circuit (Figure 9, 62) receiving an interchange control signal for interchanging, in the memory cell array, information held in the first information holding circuit and information held in the second information holding circuit with each other (Column 1, lines 60-68, Column 2, lines 1-28).

Allowable Subject Matter

11. Claims 2-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-36 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ooi (U.S. Patent No. 5,043,878), Yamaguchi et al. (U.S. Patent No. 4,947,373), Dolkas et al. (U.S. Patent No. 5,007,051), Taniai et al. (U.S. Patent No. 5,043, 935), and others, does not teach the claimed invention having the transistor circuit of the first port section is formed by transistors of a threshold voltage and the transistor circuit of the second port section is formed by transistors of a different threshold voltage, and wherein a power source voltage supplied to the first port section and that supplied to the second port section are different from each other.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le Primary Examiner

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